Jk flip flop operation pdf

A positive clock transition allows you to switch the output Q. The state of enable does not last throughout the entire positive phase of the hour. Only J&K entries cannot cause a transition, but their values at pgt time determine the output according to the truth table. This is the application of versatile J-K flip-flops. Because this 4-NAND version of J-K flip-flops is subject to a racing problem, the Master-Slave JK Flip Flop has been developed to provide a more stable circuit with the same function. Master-Slave JK Flip Flop has two closed SR loafers that are used as bolts in a way that suppresses race or racing behavior. Another way to look at this circle is like two J-K flip-flops tied together with another driven reverse clock signal. When the clock makes a positive transition, the main part is activated, but the slave part is not because its clock is reversed. In the half-cycle of the hour, on the downward transition, the reverse clock has a positive transition and triggers the slave part. The final output Q then monitors the output of main Part M after half a cycle of the hour. The JK flip-flop is a sequential bi-state single-bit memory device named after its inventor Jack Kil. In general, there are one clock pin (CLK), two data entry pins (J and K) and two output pins (Q and Q)) as shown in Figure 1. JK flip-flop can be activated at the leading edge of the watch or on the accompanying edge and can therefore be positive or negative. JK Flip Flop CircuitIn in order to have an insight into the operation of jk flip-flops, must be realized in terms of basic doors similar to those at number 2 expressing JK flip-flop with a positive edge using both doors and NOR doors. It is shown here that exit Q is logically ied with the k input and the clock pulse (using I gate 1, A1) while the output Q is with both the J input and the clock pulse (using I gate 2, A2). Furthermore, exit A1 is fed as one of the entrances (X1) to NOR gate 1, N1 whose second entry (Y1) is connected to the output Q1. Similarly NOR door 2, N2 has its own two inputs (X2 and Y2) as output A2 and exit Q (respectively). Initially let J = K = 0, Q = 0 and Q=1. Now consider the appearance of a positive edge of the first heart rate of the watch on the CLK pin of the flip-flop. This results in X1 = 0 and X2 = 0. Then the output N1 will become 0 as X1 = 0 and Q&=1; while the N2 output will become 1 as X2 = 0 and Q = 0. Thus you get Q = 0 and Q¢= 1.However, if the initial states are considered J = K = 0, Q = 1 and Q¢= 0, then X1 = X2 = 0 resulting in Q = 1 and Q¢= 0. This means that the state of flip-flop outputs Q and QO remains unchanged in case J = K = 0.Now assume that J = 0, K = 1, Q = 0 and Q¢= 1. By analysing on the same grounds, X1 = X2 = 0 is obtained which further results in Q = 0 (and therefore Q¢= 1). For the same case Q and Q are 1 and 0, respectively, X1 = 1 and X2 = 0 resulting in Q = 0 (and therefore Q¢= 1). This implies that if J = 0 and K = 1, then the flip-flop resets (Q = 0 and Q¢= 1). Then if J = 1, K = 0, Q = 1 and Q¢= 0, then X1 = X2 = 0 resulting in Q = 1 (and so Q¢= 0). For the same case if Q = 0 and Q¢= 1, then X1 = 0, X2 = 1 leading to Q¢= 0 and therefore Q is forced to appreciate 1. This means that in case J = 1 and K = 0 flip-flop output will always be set respectively Q = 1 and Q¢= 0.Similar to J = 1, K = 1, Q = 1 and Q=0 one gets X1 = 1, X2 = 0 and Q = 0 (and therefore Q=1); and if Q changes to 0 and Q0 to 1, then X1 = 0, X2 = 1 that forces Q to 0, and therefore Q to 1. This means that for J = K = 1, flip-flop outputs change, which means that Q changes from 0 to 1 or 1 to 0, and these changes are reflected on the output pin Q accordingly. However, it should be noted that the state of flip-flops remains unchanged if there is no rise-edge watch on its intake. JK Flip Flop Truth TableSamiti table for JK flip flop is summarized in table I below. Wave forms relating to the same are presented on 3. Moreover, it should be noted that the operation of the loafers with a negative edge is similar to that of the positive edge, except that the changes occur at the accompanying edge of the pulse of the clock instead of its leading edge. JK Flip Flop Timing DiagramFrom the truth table above you can get to the equation to exit the J K flip-flop as (Table II). This is known as a time diagram for JK flip-flop. In addition to the basic input-output pins shown in Figure 1, J K flip-flops may also have special input data such as clear (CLR) and preset (PR) (Fig. 4). They can be used to bring flip-flops to a certain state from the current state. For example, the output can be equated to 0 using a CLR pin, while it can be set to 1 using a PR pin. However, these pins may be active high (Fig. 4a) or active low (Figure 4b) managed. Wave forms relating to JK flip-flops with positive edges with active high pre-set and clear needles are shown in Figure 5.Moreover, it should be noted that these needles may be either synchronous or asinchronous in nature, which means that clear and set operations occur depending on the clock (shown by green lines) or not (shown by red lines). Furthermore, if preset and clear needles are actively low, the changes observed in the diagram occur at a time when they are clear and preset low instead of high. There are also D Flip-flops, SR flip-flops, active low-sr flip-flops and Gated SR flip-flops. You can learn more about JK loafers and other logical doors by checking our full list of logical door questions. After studying this section, you should be able to: Understand JK Flip-flop circuits and can: • Describe typical applications for JK flip-flops. • Identify standard circle symbols for JK flip-flops. • Identify JK Flip-flop integrated circuits. Describe alternative forms of JK flip-flops. Understand time diagrams to explain the work of JK flip-flops. Use software to simulate JK flip-flops. JK Flip-flop is also called a programmable flip-flop because, using its inputs, J, K, S and R, it can be made to mimic the action of any of the other types of flip-flops. Fig 5.4.1 displays the basic configuration (without input S and R) for JK flip-flop using only four NAND doors. The circuit is similar to the SR flip-flop clock shown in Fig. 5.2.7, (Digital Electronics Module 5.2), but in Fig. 5.4.1, it can be seen that although the clock input is the same as in the SR flip-flop, the NAND 1 door in Fig. 5.4.1 is now three front doors, and the set input (S) has been replaced by an entry marked J. 5.4.1 now has three front doors and the set entrance (S) has been replaced by an entry with A. , and the third entry provides feedback from the Q output. The NAND 2 reset input (R) from Fig. 5.2.7 has been replaced by input K and there is an additional feedback link from Q. The purpose of this feedback is to eliminate the indefinite state that occurred on the SR flip-flop when both entries were made by logic 0 at the same time. Operation As a starting point, assume that both J and K are in logic 1 and exits Q = 0 and Q = 1, this will cause nand 1 enabled, because it has the logic of 1 on two (J and Q) of its three inputs, requiring only logic 1 on its input clock to change its output state to logic 0. At the same time, NAND 2 is disabled because it has only one of its inputs (K) on logic 1, its feedback entry is in logic 0 due to feedback from Q. Upon arrival of the clock heart rate, the output of NAND 1 therefore becomes logic 0 and causes the Japanese to change the state so that Q = 1 and Q = 0. This action enables NAND 2 and disables NAND 1. However, as this change occurs at the exits, there is a problem. If the clock's heart rate is still high, or in the period while the flip-flop changes, the OUTPUT of NAND 2 will immediately go to logic 0 and the flip-flop will reset back to its original state. It can then set up a situation in which the flip-flop will quickly oscillate between her two countries. These problems caused by output data racing around the return lines from the exit to the entrance before the end of the hour are known as RACE HAZARDS and must of course be avoided. However, this can be done using a more complex version of the circle. In addition to minimizing the problems with race hazards, this type of flip-flop can also function as sr, SR with clock, D type or toggle flip-flop. The terminology of the slave master refers to a device that has two separate stages of flip-flops, isolating the entrance from the exit. In addition to reducing the problem of race risk, it also has an additional advantage over simpler SR types, as its J and K inputs can be any value without causing an unspecified state. The typical circle symbol is shown in fig. 5.4.2, and Table 5.4.1 shows how different combinations of logic applied to J and K inputs change the way JK flip-flops the clock heart rate at the CK input. • When J and K 0 flip-flop is inhibited, Q is the same after ck heart rate as it was before; there is no change on the exit. • If J and K are at different levels of logic, after ck heart rate, Q and Q will take up the same states as J and K. For example, if J = 1 and K = 0, then at the accompanying (negative going) edge of the heart rate of the clock, Q output will be set to 1, and if K = 1 and J = 0 then the Q output is reset to logic 0 on the accompanying edge of the clock , effectively mimicking the D type of master rob flip-flop by replacing the D input with J. • If logic 1 applies to both J and K , the output switches on the accompanying edge of each clock pulse, just like the toggle flip-flop. JK flip-flop can therefore be called 'programmable flip-flop' because of the way its operations can be programmed by J and K states. Each of the above actions is synchronized with the pulse of the watch, the data is taken to the main flip-flop on the growing edge of the clock pulse, and the exit from the slave flip-flop appears at the drop-off edge of the clock pulse. For example: Although the above describes the effect of master glory JK flip-flops, both positive edge and negative edge-induced versions are available. Asinchronous Inputs Asynchronous inputs, which act independently of the heart rate of the clock, are also provided by active low intakes of PR and CLR. They act as (usually active low) SET and RESET input devices, and how they operate independently of the clock input, give the same content as a simple SR flip-flop. As with sr flip-flop, in this mode, an external method is required to ensure that these two inputs cannot be active at the same time, as both Q and Q logic 1 would do. The theoretical schematic circuit level diagram prompted by jk master rob flip-flop is displayed in Fig. 5.4.3. Gates G1 and G2 form a similar function as the front door in the basic JK flip-flop shown on Fig 5.4.1, with three inputs to allow back-up links Q and Q. Gates G3 and G4 form the main flip-flop and the G7 and G8 doors form a slave flip-flop. Two more gates, the G5 and G6, are included between the master and the goods for the transfer of data from master to slave. The way this transmission occurs is that the output of the main flip-flop is delayed for the duration of the clock's heart rate, by temporarily stored in the main flip-flop, while the CK pulse is high. The operation (in fold-out mode) is as follows: Loading the Master Flip-flop with J and K and on logic 1 (transfer mode setting), suppose that Q = 0 and Q = 1, door G2 will be disabled because, although there are two logical 1 countries on their J and CK inputs, the return (lower) G2 entry will be on logic 0 due to feedback from Q. G1 , however , it has the logic of 1 coming back from Q , which ensures that the G1 door is enabled, because all three of its inputs are now logic 1. Exit G1 will therefore be in logic 0 (NAND door rules), which will master flip-flop (G3 and G4) set your q1 output to logic 1, and q1 output to logic 0. Over time CK input remains on logic 1, q1 and q1 will remain at q1 = 1 and q1 = 0, but the transmission doors G5 and G6 are inhibited because for example, if Q is currently on logic 0 and Q is on logic 1, door G1 will have all three of its inputs on logic 1, so its production will be 0. Since the G1 output is also an active low SET entry G3, as ck pulse went to logic 1, the G3 output went to logic 0, setting the main flip-flop output q1 to logic 1. Transmission door control Logic 0 at exit G1 will cause the G5 transmission door to be disabled, and in combination with logic 1 to q1 this will cause the G5 output to remain on logic 1 for the duration of the CK heart rate. However, the G6's contribution from the G2 exit will be on Logic 1, but as Q1 will now be on logic 0, the G6 transfer gate will also be disabled, which will make its exit logic 0. Data at q1 and q1 exits will therefore not be passed on to the slave flip-flop for the duration of the clock pulse. Clock Pulse drops edge After the clock input goes low however, logic 0 is applied to the clock entry gate G1 and G2. The G1 exit now returns to logic 1, making both the entrances to the doors of G5 logic 1, and causing its production to fall to logic 0. With q1 still on logic 0, the G6 door is still disabled, so the G6 exit is on logic 1. Rob flip-flop With exit gate G5 on logic 0 and G6 output on logic 1, doors G7 and G8 are set, which form a low-activated SR flip-flop, and so Q becomes logic 1 and Q becomes logic 0. The exit conditions are now reversed, and this change is returned to the G1 and G2 front door. However, these are now both disabled because the clock intake is already low, so it does not affect the main flip-flop. The arrival of the rising edge of the next heart rate of the watch then allows for new levels of logic on Q and Q in return entries to the G1 and G2 door as before, but this time Q is on logic 1, so the G2 door will be enabled at the growing edge of the clock pulse. Now, as the heart rate of the clock goes to logic 1 the main flip-flop will reset, q1 will go to logic 0 and at the drop-down pulse of the clock the transmission gate will pass the data to the slave loafers by placing Q back to logic 0, so that Q and Q come out once more. Although the standard JK flip-flop circuit shown in Fig. 5.4.3 works, the switching of the transfer door limits the operation of the circuit to the starting level. However, in 2014, the 5.4.4 illustrates a different method of transferring data from master to slave flip-flop. Instead of the G5 and G6 transmission doors used in Fig. 5.4.3, Fig. 5.4.4 uses the NOT door to reverse the positive CK pulse that triggers the main flip-flop, producing a reverse version of the clock pulse to trigger the slave flip-flop. With this modification data, it is imminted in the main flip-flop on the growing edge of the CK entrance. It was Changes in data to J or K now do not affect the state of the main flip-flop while CK is high, as feedback from Q and Q will always disable which of the two front doors could make a change in the main Japanese. Because of the CK inverter, on the falling edge of the CK pulse, the slave flip-flop now sees a growing edge, and the slave flip-flop accepts data from q1 and q1 that jars states Q and Q. This main circle of slaves therefore accepts only data from J and K on the growing edge of CK and exits them to Q and Q on the falling CK edge. However, in both figs. 5.4.3 and 5.4.4 master and rob flip-flops are both simple levels powered by clock SR flip-flops. Both designs work as intended for JK flip-flop, in switch mode. However, in modes where J and K can be changed, the main flip-flop in Fig. 5.4.3 accepts data from inputS J and K whenever the CK heart rate is high, allowing the main flip-flop outputs to change as long as the CK heart rate is high. Therefore, these are the data that are present at the moment before the fall of the CK edge, which is transmitted to the slave flip-flop. In the like. 5.4.4 The main flip-flop only accepts data on the growing edge of CK and releases this data at the falling edge of ck pulse. Although the slave flip-flop is also activated, it will not change after the clock entry is low, as its input is taken from the exit of the main flip-flop, which will not accept changes due to low clock input. Fig 5.4.5 shows a positive edge triggered by a JK flip-flop (not the main slave) built from the positive edge triggered by the D Type flip-flop, which uses a modified data select circuit to correctly direct feedback from Q and Q outputs to the J and K inputs. This circuit also uses asinchronous SET and RESET input D Type flip-flops, and since the D Type is running, this version of JK loafers is indeed a edge (not level) activated. It is also possible to use a negative edge triggered by the D Type flip-flop to make a negative edge triggered by jk flip-flop by this method. Fig 5.4.6 displays the JK Master Slave Flip-flop using two positive edges launched D Type flip-flops and reversed the heart rate of the watch to turn the slave flip-flop into a negative edge trigger. This design therefore has a real edge that triggers both the lifting and falling edges of the clock heart rate and is immune to any changes in data that occur during periods of high or low hour signal levels (except for any changes or disturbances that may occur during the Tsetup or thold period near the edges of the clock heart rate, as described in Sequential Logical Module 5.3). 5.3).